

D) AMENDMENTS TO THE DRAWINGS

Applicant has attached a Replacement Sheet and an Annotated Marked-up Drawing, including proposed new Figure 14A, and Figure 14.

REMARKS

This is a Response to the Office Action dated June 30, 2005. Upon entry of this Response, Claims 11-35 and 42-43 will be pending in this Application.

In the outstanding Office Action, the Examiner withdrew from consideration claims 36-41; objected to Claim 18; rejected under 35 U.S.C. 112, second paragraph, claims 11, 24, 32, 34 and 35 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; objected to claims 26-27 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form; rejected claims 11-25, 28-34, and 42-43 under 35 U.S.C. 103(a) as being unpatentable over Takada et al. (US 6278813); objected to the drawings; and requested affirmation of a provisional election made by telephone on June 21, 2005 by William P. Smith.

Allowable Subject Matter

The Examiner objected to Claims 26-27 as being dependent upon a rejected base claim, but indicated that these two claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if the base claim of these claims is no longer rejected under 35 USC 112. Applicant appreciates the Examiner's provisional indication of allowability of Claims 26-27, but for the reasons set forth below, Applicant believes that all of the claims are allowable.

Election Requirement

Applicant confirms the election of the claims and cancels Claims 36-41 without prejudice.

Claim Objections

Claim 18 has been amended to address the Examiner's objection.

Claim Rejections - 35 USC §112

Claims 11, 24, 32, 34 and 35 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant also notes that the only basis for rejecting claim 35 was the reason set forth under 35 U.S.C. §112, 2nd paragraph, so that claim 35 would be allowable if amended to overcome the rejection under §112. Applicant respectfully traverses the rejection of claims 11, 24, 32, 34 and 35 under 35 U.S.C. 112, second paragraph.

Specifically, the Examiner stated:

"Claim 11 recites the limitation 'said plurality of arrayed waveguides' in the 4th parag. of the claim. There is insufficient antecedent basis for this limitation in the claim. Correction is required.

Claim 35 recites the limitations 'the modulator block' in the 2nd line of the claim. There is insufficient antecedent basis for this limitation in the claim. Correction is required. Claims 24, 32 and 34-35 are ambiguous, since 'waveguide amplifier block' is 'a 'waveguide amplifier block' and the claim language implies that 'the waveguide amplifier block is configured for connecting an external pump laser with the waveguide amplifier block through a wave guide interconnect' there are two separate elements 'waveguide amplifier block' and 'waveguide amplifier block'; also the analogous comparison of discrepancies is between an 'active unit' and a 'modulator block' as being separate units as claimed in claim 32; also the analogous comparison of discrepancies is between an 'photonic integrated circuit' and 'active unit' and/or 'the modulator block' as being separate units as claimed in claims 35 and 34. Corrections are required."

Applicant has amended the claims in way that is believed to overcome the Examiner's rejections. Further, with respect to claims 34 and 35, the photonic integrated circuit, active unit and modulator block are indeed separate units. To the extent that the Examiner's rejection implies that the claiming of those elements as "separate units" is a discrepancy, Applicant points out that the use of two or three cascaded units is shown in Figures 13 and 14, and described in paragraphs 69 and 70 of the amended specification. Therefore, claiming the elements as separate units is intentional and is supported by the specification.

Objections to the Drawings

The Examiner stated that the modulator for electro-optically processing output signals, as claimed in claim 28, which depends on claim 27, must be shown or the feature(s) canceled from the claim(s).

A proposed new Figure 14A is attached hereto, which is essentially the same device as shown in Figure 14. Figure 14A shows the device with the input signal into the Amplifier Block, and the output from the modulators 206. There is no difference in both Figures, it is simply a matter of which interface is selected as the input.

Applicant points out that in paragraph 66 of the substitute specification, there is support for a modulator for electro-optically processing output signals. Specifically, paragraph 66 states as follows:

" The third phase of integration will allow combining these low-loss PICs with active elements such as laser-diodes or VCSELS, detector arrays, and electro-optic modulators to produce a line of optronic modules and systems. Examples include, multi-channel modulators, receivers, transmitters, transceivers and transponders, and fully built out DWDM systems."

Thus, the electro-optic modulators are not limited to the input of a third-phase integrated circuit. Moreover, the placement of a modulator at an input or output is irrelevant, the output signal will be modulated if the modulator is positioned at the input of the RAWG, or if it is positioned after, for example, an amplification stage. Therefore, Applicant respectfully submits that the specification provides support for the device of claim 28, which in pertinent part states: "a signal processing unit coupled to the photonic integrated circuit for electro-optically processing the input and output signals."

Claim Rejections - 35 USC §103

The Examiner rejected Claims 11-25, 28-34, and 42-43 under 35 U.S.C. 103(a) as being unpatentable over Takada et al. (US 6278813). Claims 11 and 23 have been amended to overcome this rejection.

Specifically, the Examiner stated:

"Regarding claim 11, 23- 24, 28-34 and 42-43, Takada teaches a second/third-phase optically integrated circuit (shown in at least fig. 24) comprising a monolithically integrated circuit (shown in at least fig. 31), comprising:

an input/output interface arranged on a substrate 1 comprising a plurality of waveguides 2 for simultaneously inputting at least one signal to and outputting at

least one signal from the monolithically integrated circuit for demultiplexing a multiplexed optical signal in to n different constituent wavelengths and for combining n input optical signals composed of n different constituent wavelengths in to a multiplexed signal (shown in at least fig. 31, see also abstract and col. 2, 2nd parag.); a slab waveguide 3 arranged on the substrate 1 having a first end and a second end, the first end coupled to the plurality of waveguides 2 of the input/output interface to focus the at least one input signal to the second end, and the second end coupled to the array of waveguides, for focusing the at least one output signal to the input/output interface through the first end (shown in at least fig. Item (sic) input/output waveguides and output signal being focused out of the slab 2nd end through output/input waveguides 2); an array waveguide 93 arranged on the substrate 1 comprising a plurality of waveguides for coupling the one or more input signals (see waveguides in the area 88), separating the one or more input signals into the n different constituent wavelengths and focusing the n different constituent wavelengths back on to the slab 3 waveguide first end coupling to the input/output interlace (shown in at least fig. 31, items waveguides coupling input light from the waveguides 2 through slab 3, and see col. 2, 2nd parag.), the plurality of waveguides of the array waveguide 93 being optically coupled at one end with the second end of the slab 3 waveguide, and terminated at the opposing end by the reflective mirror 87, each waveguide of said plurality of arrayed waveguides 93 having a predetermined path difference between successive waveguides (shown in at least fig. 31, items waveguides with different predetermined wavelengths), a reflective mirror 86 disposed at the opposing end of the array waveguide 93 for reflecting the one or more signals incident on it from the array waveguide 93 back into the array waveguide 93; and an active unit 22 formed on the substrate, the active unit connected to the photonic integrated circuit by a waveguide interconnect means (see at least col. 29, 1st parag and col. 3, lines 38-43; wherein active unit is an array of photodiode formed on a perspective output waveguide array); a signal processing unit comprises a plurality of n electro-optical elements coupled to the photonic integrated circuit for electro-optically processing the input and output signals (see fig. 53, item signal processing elements/unit(s) 22 and/or 23);

However, Takada does not explicitly state that the above monolithically integrated circuit is a photonic integrated circuit; and that the above active unit is a waveguide amplifier and that the above signal processing unit is a modulator for interconnecting to an external optical device/pump laser. It is well known to those of ordinary skill in the art when the invention was made that a monolithically integrated circuit is known as a photonic integrated circuit and that it would have been obvious to a person of ordinary skill in the art when the invention was made to choose the above active device as a mater of further modification of signal an optical amplifier since such amplifier on an AWG circuit is conventional and that it would have been obvious to a person of ordinary skill in the art when the invention was made to externally connect the above integrated circuit/RAWG to any external optical and/or non-optical device, such as a modulator or laser source, as a mater of further analyzing or processing the signal and since such interconnections are conventional, see the prior art of the record, and also

suggested/implicit by various embodiments by Takada, and since such optical integrated circuit enables accurately input/output desired frequencies and provide measurement without any loss (col. 11, 1st parag.)."

Applicant notes that claims 11 and 23 have been amended to overcome the rejection to include an integral mirror, all of the dependent claims being dependent from these two independent claims and therefore including this limitation. Takada does not teach or suggest an integral mirror, and specifically teaches away from a monolithically integrated mirror (See *e.g.*, Col. 22, lines 25-62). Applicant further notes that Takada is distinguishable from the present invention. Applicant respectfully traverses the Examiner's rejection of claims 11-25, 28-34, and 42-43 under 35 U.S.C. 103(a).

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In *re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. In *re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In *re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)."

See MPEP §2143.03

With respect to claim 11, the device claimed in claim 11 (and in claims 12 – 22), is not a second- or third-phase photonic circuit, as indicated by the Examiner. Claim 11 is directed to the fundamental building block upon which the second- and third-phase photonic circuits are constructed.

The relevant portion of Takada discussing a circuit having a reflective mirror is set forth as follows:

"FIGS. 31 and 32 show a first and a second embodiments of arrayed waveguide optical multi/demultiplexing circuits preferred as wavelength division multi/demultiplexing circuits used for the wavelength division multi/demultiplexer according to this invention. In the embodiment in FIG. 31, parallel areas 88 and 91 in which the arrayed waveguides are parallel with one another are installed in the AWG, and a reflecting plate 86 is installed in a groove crossing each arrayed waveguides in the vertical direction, and the branching section 3 functions as a branching section. In the embodiment in FIG. 32, the parallel area 88 and a parallel area 92 in which the arrayed waveguides are parallel with one another are installed in the AWG, the reflecting plate 86 is

installed in a gap crossing each arrayed waveguides in the vertical direction, and the branching section 3 functions as a branching section. In this case, a reflecting surface 87 of the reflecting plate 86 contacts each arrayed waveguide. The length between adjacent arrayed waveguides in the AWG and the design values for the branching section thereof are the same as in the AWG shown in FIG. 1. Light input on one of the group of light input ends 2 is distributed to each arrayed waveguide by the branching section. The distributed beams propagate through each arrayed waveguide in the order of the parallel area 88, a diverging region 89, a converging region 90, the parallel area 91 (FIG. 31) or parallel area 88, the diverging region 89, the converging region 90, the parallel area 92 (FIG. 32). The beams are then reflected by the reflecting plate 86 installed in the parallel area 91 or 92 and again propagate through each arrayed waveguide in the opposite direction. The propagated beams are mixed by the branching section 3 and then distributed to each light output end. The difference in optical-path length among the arrayed waveguides of the AWG is determined by the diverging region 89 and the converging region 90, so no extra difference in optical path occurs as long as the reflecting plate is installed in the parallel area perpendicularly to each arrayed waveguide."

Takada et al., Col. 22, lines 25-62 [Emphasis added]

Takeda et al. discloses an optically integrated circuit using a mirror, in Figures 31-33, that is "installed in a gap crossing each arrayed waveguide" (Col. 22, lines 30-40). The reflective mirror is not used by Takada et al. to reduce the length of the AWG by half, as the reflective surface is in Applicant's invention. Moreover, the installation of a separate piece – i.e., a mirror – means that the Takada piece is not a monolithic device. While the reflective piece of Takada is inserted on the same substrate as the AWG, it is not monolithically integral to the AWG, as the Examiner seems to infer.

Applicant's invention is distinguishable from Takada. Placement of the mirror along the edge of the integrated circuit at a midpoint, adjacent to the region defined by Takada as the "divergent region" of the array waveguide, permits Applicant to reduce of the length of the array waveguide by half. Takada discloses a reflective array waveguide having two parallel regions 88 and 91, in which the array waveguides are parallel with one another, and further requires the two parallel regions 88, 91 to be parallel to each other, in order for the adjacent arrayed waveguides to maintain the length and design values for the branching section the same as in the prior art (Fig. 1). In order to achieve the parallel regions, as recited in Takada, the arrayed waveguide must turn at least 180°. Takada also has a divergent region 89 and a convergent region 90 connecting the path between the parallel regions. Takada is clearly distinguishable from

Applicant's disclosed configuration, which includes only one divergent region and one "parallel" region – i.e., the origination point at the slab waveguide, and has a bend radius of 90° or less in the arrayed waveguide between the slab waveguide and the reflective mirror. In fact, in Takada, all of the array waveguides shown in Figures 1-53 include two parallel regions, a divergent and a convergent, which distinguishes Applicant's invention from Takada and the prior art set forth therein.

As can be seen by comparing Figures 31 – 35 of Takada, et al., to Figures 3 and 5 in the present application, the length of the array waveguide between the slab and the reflective mirror is at least doubled in Takada et al., when compared to the length of the array waveguide of the present invention. In Takada, the light beams must proceed through at least two parallel regions, a divergent and a convergent region, which is at least double the length of Applicant's waveguide, and which effectively quadruples the distance with the light beam must travel, since the reflected light beams must propagate back again through the a waveguide that is twice the length. This waveguide configuration provides significant benefits over Takada. By effectively reducing the length of the array waveguide by approximately half that of Takada, and the light propagation distance to one-quarter of the propagation distance of Takada, Applicant's circuit significantly reduces signal losses. Signal losses are proportionate to the length of the array waveguide. The half-length waveguide also reduces the physical size of the overall chip, which permits almost double the yield per wafer for the Applicant's RAWG, compared to a TAWG having the same number of channels as the RAWG. The higher yield in turn lowers the production cost of the devices while it simultaneously enhances performance.

Applicant's reflective mirror is purposely positioned along the edge of the integrated circuit, to truncate the array waveguide at the mid-point or divergent region. By so positioning the mirror, Applicant's integrated circuit requires only half the length of waveguide array, compared to the full-length AWGs of Takeda et al. Further, the reflecting plate of Takada et al. is not a salient part of the monolithic design, rather it's an additional piece "installed in a groove..." (Col. 22, line 30-34) Applicant's invention, by contrast, has the reflective mirror integrally disposed and formed along an edge of the substrate, to permit the reflective surface to be applied directly on the monolithic circuit, so as to maintain the monolithic integration of reflective mirror, rather than having to cut a groove or gap and insert an additional piece

internally in the circuit. Monolithic integration of the mirror material by evaporative technique is deliberately employed to reduce the size of the AWG in half, yet achieving a lower loss compared to prior art.

Claims 11 and 23 have been amended to clarify that the reflective mirror is integrally formed on the edge of the chip, at the opposite end of the array waveguide. Applicant therefore submits that the photonic integrated circuits of claims 11 and 23, as amended, are not rendered obvious by Takada et al.

With respect to claims 23- 24, 28-34 and 42-43, Applicant submits that these claims are distinguishable from Takeda et al. Claim 23 is distinguishable for the reasons set forth above with respect to Claims 11 and 23. Claims 24, 28-34, and 42-43 are believed to be allowable as depending from what Applicant believes to be allowable claims 11 and 23.

Furthermore, claims 23- 24, 28-34 and 42-43 are directed to second- and third- phase, monolithically integrated circuits. Takeda et al. does not disclose interconnecting the second phase element, or the second and third phase elements, using a waveguide interconnect. To the contrary, Takeda et al. discloses interconnecting various AWGs using optical switches, which are distinct from the integration scheme of Applicant's invention. Integration by waveguide interconnect is a completely different technology with advantage over optical switches. The switches in Takeda et al. are active elements in an optical circuit. Switches are mechanical or similar devices. In several configurations, e.g., Figs. 20, 21, 25 and 28, Takada uses an array of Mach Zehnder interferometers, which are apparently integrated on the same chip as the AWG. The Mach Zehnder interferometers, however, are also switch-like devices, which are controlled using heat to switch states. In either case, whether with Mach Zehnder type switches or optical switches, their function is to turn a circuit on or off. A switch can only be in one of two states, whereas a waveguide interconnect allows continuous operation in both directions. A switch must have a mechanism for turning it ON and OFF for its functionality. However, the waveguide interconnect of Applicant's invention does not need such a mechanism. Switches have much greater loss compared to waveguide interconnects. Therefore, the integration of second phase or second and third phase elements using waveguide interconnects in a monolithic photonic integrated circuit is not anticipated by Takada.

Neither does Takada provide a second- or third-phase integration with an on-chip – i.e., monolithic - amplifier or modulator. Takada discloses only first-phase integration, which includes cascaded AWGs, e.g., Figs. 47 and 48, which the Examiner may be incorrectly assuming to be multiple phases. However, the AWGs are passive units. Takada does not disclose waveguide interconnects between AWGs and amplifiers or other active units. To the contrary, Takada teaches away from waveguide interconnects, as the active units disclosed in Takada –e.g., photodetectors 22 - are described as being directly connected to the light output ends, which indicates a connection that is not integral to the device.

The Examiner's comments indicate that he considers the substrate referred to in Takada to be the same as Applicant's substrate for forming the monolithic integrated circuit. In fact, that is not the case. Takada refers to substrate in another aspect, wherein multiple devices may be interconnected on a common backplane or substrate, such as on a PC board. E.g., in Figure 48, the description indicated that multiple devices – i.e., discreet elements - may be produced on a common substrate. See, e.g., Col. 29, lines 5-20. In a few specific instances, e.g., the Mach Zehnder configurations described in Figures 20 – 22, Takada indicates that a device is integral with the substrate, which is the sense in which the Applicant is referring to as monolithic. However, in Takada, none of the multi/demultiplexing circuits having the reflective mirror is combined with any other devices on a common substrate. See, e.g., Figures 31-35.

Applicant therefore submits that the photonic integrated circuits of claim 23, as amended, and claims 24, 28-34 and 42-43, are not rendered obvious by Takada et al.

With respect to claims 12-22 and 25, the Examiner stated as follows:

"Takada further teaches wherein the active unit is selected from the group consisting of laser diodes, VCSELS, detector arrays and electro-optic modulators, receiver, transmitter, transceivers, and transponders (see at least col. 13, line 53; wherein also it is obvious to choose a frequency channel as a matter of choice); wherein any one of the waveguides of the input/output interlace plurality of waveguides provides an input channel and a different waveguide of the input/output interlace plurality of waveguides provides an output channel (shown in at least fig. 31, 33 and 21, items waveguides of input/output channel(s)); see also at least col. 25, last parag.+); wherein any one of the waveguides of the input/output interlace plurality of waveguides provides an input channel and the remaining waveguides of the input/output interlace plurality of waveguides are

automatically output channels (shown in at least fig. 33, items waveguides of input/output/automatically output channels); wherein any one of the waveguides of the input/output interlace plurality of waveguides provides an output channel and the remaining waveguides of the input/output interlace plurality of waveguides are automatically input channels (shown in at least fig. 33, items waveguides of input/output/automatically output channels); wherein the one waveguide of the input/output interlace is preselected as an input channel (shown in at least fig. 33, items waveguides of input/output preselected as input/output channel); wherein one of the plurality of waveguides of the input/output interlace is an input and the remainder of the waveguides form output channels (shown in at least fig. 33, item #1 waveguide and output waveguides), and the number of output channels is n wherein n is selected from one of the group of integer numbers consisting of 4, 8, 12, 16, 24, 32, and 48 (see at least fig. 33, item Array waveguide grating 19 output with 4 output waveguides; wherein it is also obvious to choose any number of channels as a matter of choice); wherein one of the plurality of waveguides of the; input/output interlace is an output and the remainder of the waveguides form input channels, and the number of input channels is n wherein n is selected from one of the group of integer numbers consisting of 4, 8, 12, 16, 24, 32, and 48 (see at least fig. 33, item Array waveguide grating 93 outputs with 1 input waveguide; wherein it is also obvious to choose any number of channels as input/output a matter of choice); wherein n waveguides of the plurality of input/output interlace waveguides are spaced at a predetermined distance and form n channels (shown in at least fig. 33, item spaced waveguides with n channels); wherein the predetermined distance is selected from the group consisting of 0.25 nanometers, 0.4 nanometers, 0.8 nanometers, 1.6 nanometers, 4 nanometers, and 5 nanometers (see at least ccl. 2, line 10; wherein it is also obvious to choose channel spacing as matter of design choice); wherein n waveguides of the plurality of input/output interlace waveguides form n channels, and the channel frequency is a predetermined frequency (see at least ccl. 8, 1st parag.); wherein the predetermined channel frequency is selected from the group consisting of about 31 GHz, and 50 GHz, 100 GHz, 200 GHz, 500 GHz, and 624 GHz (see at least col. 13, line 53; wherein also it is obvious to choose a frequency channel as a matter of choice)."

Applicant respectfully traverses the Examiner's rejection of claims 12-22, and 25. To begin, claims 12-22 depend from independent claim 11, and claim 25 depends from independent claim 23. Applicant believes that currently amended claims 11 and 23, are allowable for the reasons set forth above, which would make the dependent claims 12-22 and 25 allowable as well.

Furthermore, the Examiner's statement that "Takada further teaches wherein the active unit is selected from the group consisting of laser diodes, VCSELS, detector arrays and electro-optic modulators, receiver, transmitter, transceivers, and transponders" is

simply not supported by the Takada reference. Indeed, with the exception of the word "detector", none of these active elements is mentioned in Takada. Photo-optic detectors are used in the Takada reference, however, the photodetectors are connected to the light output ends and not integrated monolithically with the AWGs, as discussed above.

The passage cited by the Examiner for Takada reads as follows:

" ch.sub.1 of the AWG 19 is 100 GHz (0.8 nm in a 1.5 .mu.m band)"

Clearly, the cited passage does not disclose any active unit.

Applicant therefore submits that the photonic integrated circuits of claims 12-22, and 25, are not rendered obvious by Takada et al.

CONCLUSION

In view of the above amendments and arguments, Applicant respectfully requests reconsideration and allowance of claims 11-35, 42 and 43. Should the Examiner have any questions, the Examiner is requested to contact the undersigned attorney. This Response is filed in response to the Office Action dated June 30, 2005. A petition for one month extension of time and the extension fee is enclosed herewith. However, in the event that fees are due, the Commissioner is hereby authorized to charge any applicable fees and credit any overpayments to Deposit Account No. 50-1059.

Respectfully submitted,



WILLIAM P. SMITH
Reg. No. 34,931

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McNees Wallace & Nurick
100 Pine Street
P.O. Box 1166
Harrisburg, Pa 17108-1166
Phone: 717-237-5260
Fax: 717-237-5300
Attorney for Applicant



Attorney Docket No.: 23634-0001
First Named Inventor: RAHMAN, Anis
Application No.: 10/605,638
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Sheet 14 of 15

ANNOTATED MARKED-UP DRAWING

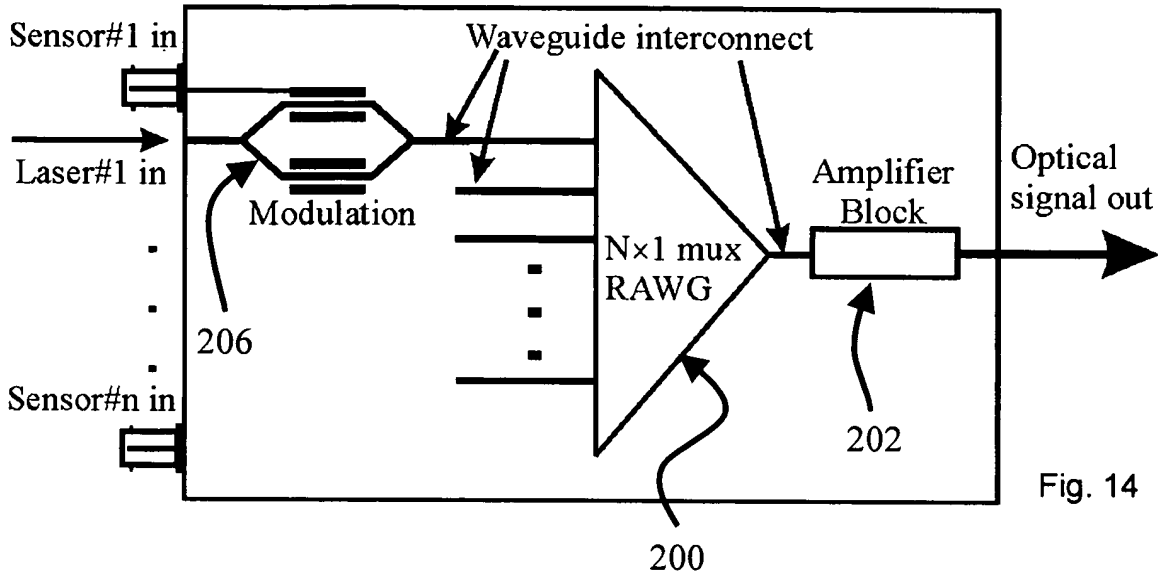


Fig. 14

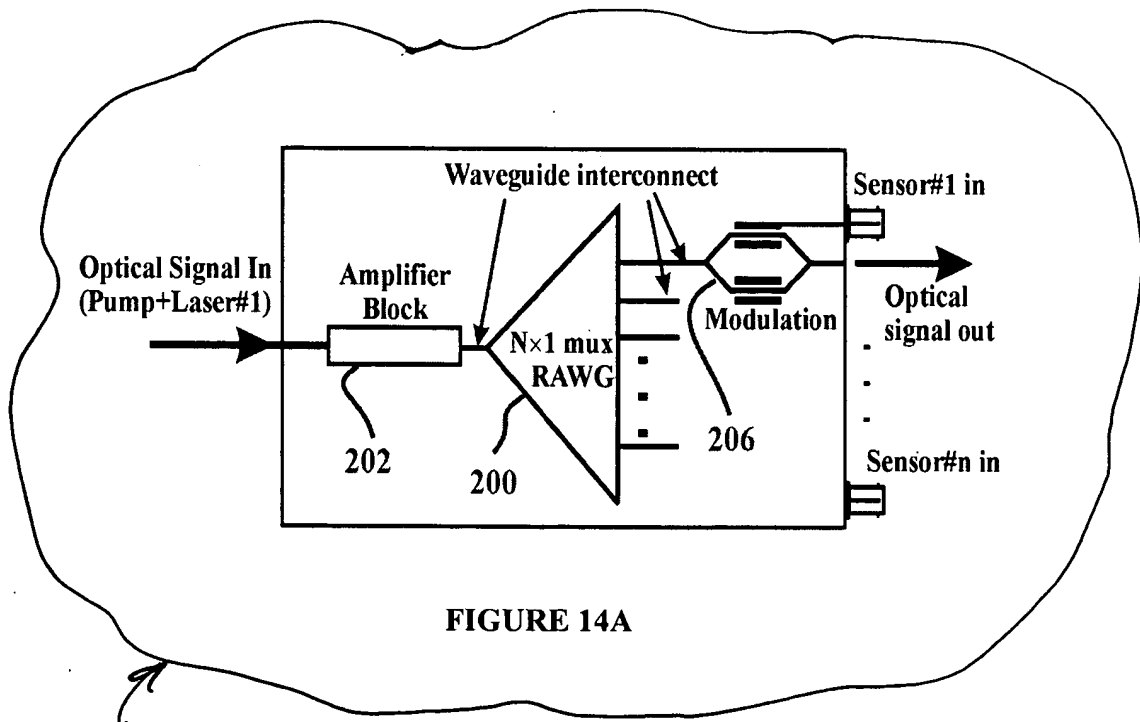


FIGURE 14A

added FIGURE 14A